REMARKS

Claims 1-15 are currently pending in the application. Claim 1 is an independent claim and claims 2-15 depend there from. Dependent claims 14-15 are currently amended to overcome a minor informality noticed by the Examiner. The Applicant respectfully asserts that the minor amendments to dependent claims 14-15 do not alter the scope of the claim as originally presented, but rather corrects a minor error objected to by the Examiner. The Applicant respectfully requests that the application be reconsidered in view of the amendment set forth above and the following remarks.

I. Claim Objections

In paragraph 1 on page 2 of the Office Action, dependent claims 14-15 were objected to for a minor informality. The Applicant respectfully traverses the objections, however, in order to advance prosecution in the application, the Applicant has amended claims 14-15 to correct the noticed minor informality. The Applicant believes the amendment to dependent claims 14-15 have indeed overcome the noticed minor informality and therefore respectfully requests that the objection be withdrawn.

II. Traversal Of Claim Rejections - 35 U.S.C. § 112

In paragraph 2 on page 2 of the Office Action, claims 1-15 were rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically, the Office Action states that the "phrase 'a transistor layer integrated within the chip' is unclear because it does not specify which layer of a transistor is 'a transistor layer.'" Further, the Office Action states that the "phrase 'at least one transistor of a first transistor type that **couples** said transistor layer to said shielding layer' is unclear" because "[i]t is unclear how the transistor of a first transistor type can couple the transistor layer to the shielding layer when the transistor of a first transistor type [is]

lying above both the transistor layer and the shielding layer." Applicant respectfully traverses the rejections for at least the following reasons.

The Applicant respectfully traverses the rejections in claims 1-15 because the specification and claims are clear as to the meaning of "a transistor layer integrated within the chip." The term transistor layer is not meant to refer to a layer of a transistor. Instead, it indicates a layer of the chip in which transistors are located. The specification states that "[t]he transistor of the second transistor type may be a n-type transistor, which may be disposed within the transistor layer." (Paragraph 11, Lines 1-2). Further, the specification states that "[t]he transistor of the first transistor type may be a p-type transistor, which may be disposed within the transistor layer." (Paragraph 11, Lines 4-6). One skilled in the art would recognize that the transistor layer is represented by 110 and 120 in Applicant's Figure 2 and is not intended to be a layer of the transistor but is a layer of the chip in which the transistors reside. In describing Figure 2, Applicant states "**[t]he NMOS transistor 90** may include, for example, a p+-body (B), an n+-source (S) and an n+-drain (D) which **may be disposed in a p-well 110**. The p-well 110 may be an isolated p-well since, for example, it may be disposed between two n-wells 120 and the deep n-well 80." (Paragraph 11, Lines 4-6) (Emphasis added). This clearly indicates that the transistor layer is not intended to be a part of the transistor but instead, is a layer of the chip in which the transistors are located.

The Applicant respectfully traverses the rejections in claims 1-15 because the specification and claims are clear as to the meaning of "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer." The specification states that "[t]he transistor of the first transistor type may be capacitively coupled to the shielding layer...." (Paragraph 11, Lines 6-7). One skilled in the art would understand the meaning of "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer" as described in Applicant's independent claim 1. Therefore, the Applicant respectfully requests that the 35 U.S.C. § 112 rejections to claims 1-15 be withdrawn.

III. Traversal Of Claim Rejections - 35 U.S.C. § 103(a)

In paragraph 4 on page 3 of the Office Action, independent claim 1 and dependent claims 8-9, 12 and 14-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Puar et al. U.S. Patent 6,356,497 (Puar) in view of McCormack et al. U.S. Patent 6,395,591 (McCormack). Applicant respectfully traverses the rejections for at least the following reasons.

Puar, even if combined with McCormack, is different from Applicant's independent claim 1. The proposed combination of Puar and McCormack at least fails to disclose a "shielding layer" as set forth in Applicant's claim 1. Puar is silent regarding a "shielding layer" as set forth in Applicant's claim 1. McCormack merely teaches an epitaxy layer. It is known in the art to form an epitaxy layer on top of a substrate surface unsuitable for fabrication. In this regard, the epitaxy layer functions as a new layer of substrate suitable for forming transistors. As stated in McCormack:

> [A] p-type epitaxy layer (p-epi) 12 is grown on the substrate 10 and a subsequent conventional twin tub process is carried out to form N-wells (20 and 22) and P-wells (16 and 18) in the p-epi layer 12. Subsequently, conventional fabrication process steps are used to form p-channel transistors (e.g. transistor 30) in the N-wells and n-channel transistors (e.g. transistors 28 and 29) in the P-wells.

(Column 2, Line 67 – Column 3, Line 7). Nowhere in the cited art does it state an epitaxy layer is used as a "shielding layer" as described in Applicant's specification. Thus, the combined references do not teach each and every limitation as set forth in Applicant's claim 1.

For at least the reasons set forth above, Applicant respectfully asserts that claim 1 is allowable over the proposed combination of Puar and McCormack. Applicant requests that the rejection of claim 1 be withdrawn.

Because dependent claims 2-15 depend, directly or indirectly, from independent claim 1, and because claim 1 is allowable over the proposed combination of references, Applicant asserts that rejections of dependent claims 2-15 are now moot. Applicant asserts that claims 2-15 are also allowable over the cited references and requests that the rejections of claims 2-15 be withdrawn.

In paragraph 5 on page 4 of the Office Action, independent claim 1 and dependent claims 2-10, 12 and 14-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar. Applicant respectfully traverses the rejections for at least the following reasons.

McCormack, even if combined with Puar, is different from Applicant's independent claim 1. The proposed combination of McCormack and Puar at least fails to disclose a "shielding layer" as set forth in Applicant's claim 1. McCormack merely teaches an epitaxy layer (as discussed above). Puar is silent regarding a "shielding layer" as set forth in Applicant's claim 1. Thus, the combined references do not teach each and every limitation as set forth in Applicant's claim 1.

For at least the reasons set forth above, Applicant respectfully asserts that claim 1 is allowable over the proposed combination of McCormack and Puar. Applicant requests that the rejection of claim 1 be withdrawn.

Because dependent claims 2-15 depend, directly or indirectly, from independent claim 1, and because claim 1 is allowable over the proposed combination of references, Applicant asserts that rejections of dependent claims 2-15 are now moot. Applicant asserts that claims 2-15 are also allowable over the cited references and requests that the rejections of claims 2-15 be withdrawn.

IV. Traversal Of Perceived Assertion Of Official Notice

The Office Action states the following:

> ... McCormack (Fig. 2) teaches the forming of a transitor within a transistor well layer, and the transistor well layer is shielded by a shielding layer 12. Accordingly, it would have been obvious to modify the device of Puar by forming the shielding layer with the structure as set forth above, because as is well known, such shielding layer would isolate the transistor from the substrate for preventing the parasitic resistance or the parasitic capacitance formed between the transistor and the substrate.

See Office Action at page 4. As noted above, the Office Action, through this statement, asserts that McCormack teaches shielding a transistor layer from the substrate using a shielding layer. The Office Action does not offer a cite from McCormack for this limitation, because no such citation exists. Instead, the Office Action summarily concludes that the epitaxy layer in McCormack is a shielding layer, and "as is well known, such shielding layer would isolate the transistor from the substrate for preventing the parasitic resistance or the parasitic capacitance formed between the transistor and the substrate."

This statement that the shielding layer was taught in McCormack and "as is well known, such shielding layer would isolate the transistor from the substrate for preventing the parasitic resistance or the parasitic capacitance formed between the transistor and the substrate," could be interpreted as the Office Action asserting Official Notice. If the Office Action is asserting Official Notice that the subject of the statement is common knowledge, the Applicants respectfully traverse the assertion as further set forth below. Alternatively, if the assertion is based on the personal knowledge of the Examiner, then under MPEP § 2144.03(C) and 37 C.F.R. § 1.104(d)(2), the assertion must be supported by an affidavit from the Examiner.

According to MPEP § 2144.03(A), Official Notice, without supporting references, should **only** be asserted when the subjects asserted to be common knowledge are "capable of instant and unquestionable demonstration as being well-known." That is, the subjects asserted must be of "notorious character" under MPEP § 2144.03(A).

The Applicants respectfully submit, however, that the subject matter of the perceived assertion of Official Notice is not well-known in the art as evidenced by the searched and cited prior art. The Applicants respectfully submit that the Examiner has performed "a thorough search of the prior art," as part of the Examiner's obligation in examining the present application under MPEP § 904.02.

Additionally, the Applicants respectfully submit that the Examiner's searched and cited references found during the Examiner's thorough and detailed search of the prior art are indicative of the knowledge commonly held in the art. However, in the Examiner's thorough and detailed search of the relevant prior art, none of the prior art taught or suggested the subject

matter of the perceived assertion of Official Notice (i.e., that the shielding layer was taught in McCormack and "as is well known, such shielding layer would isolate the transistor from the substrate for preventing the parasitic resistance or the parasitic capacitance formed between the transistor and the substrate"). That is, the Examiner's thorough and detailed search of the prior art has failed to yield any mention of this statement that the Examiner implies is widely known in the art. The Applicant respectfully submits that if the subject matter of the perceived assertion of Official Notice had been of "notorious character" and "capable of instant and unquestionable demonstration as being well-known" under MPEP § 2144.03(A), then the subject matter would have appeared to the Examiner during the Examiner's thorough and detailed search of the prior art.

If the Examiner had found any teaching of relevant subject matter, the Examiner would have been obligated to list the references teaching the relevant subject matter and make a rejection. Consequently, the Applicants respectfully submit that the cited references do not teach the subject matter of the perceived assertion of Official Notice and respectfully traverse the perceived assertion of Official Notice.

The Applicants specifically challenge the Examiner's assertion of Official Notice with regard to the assertion that the shielding layer was taught in McCormack and "as is well known, such shielding layer would isolate the transistor from the substrate for preventing the parasitic resistance or the parasitic capacitance formed between the transistor and the substrate." Again, neither McCormack or Puar teach or suggest a "shielding layer." Because neither reference teaches or suggests this limitation, the Applicants assume that the Examiner must be asserting Official Notice with respect to this limitation.

As stated above, the Applicants respectfully traverse the perceived assertion of Official Notice and submit that the subject matter is not of such "notorious character" that it is "capable of instant and unquestionable demonstration as being well-known." Under MPEP 2144.03, the Examiner is now obligated to provide a reference(s) in support of the perceived assertion of Official Notice if the Examiner intends to maintain any rejection based on the assertion of Official Notice. Additionally, the Applicants respectfully request the Examiner reconsider the

assertion of Official Notice and provide to the Applicants any basis for the perceived assertion of Official Notice. If the Examiner has any questions, the Examiner is invited and encouraged to contact the Applicant at the number below for further discussion.

CONCLUSION

Based on at least the foregoing, Applicant believes that claims 1-15 are in condition for allowance. The Examiner is kindly invited to contact the undersigned at the telephone number listed below to discuss the rejection of the claims and passing such claims to allowance prior to taking any other action on the merits.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

A Notice of Allowance is courteously solicited.

Dated: November 9, 2005

Respectfully submitted,

Ronald Spuhler

Ronald H. Spuhler
Reg. No. 52,245

McAndrews, Held & Malloy, Ltd.
500 W. Madison St., 34th Floor
Chicago, IL, 60661
(312) 775-8000